## REMARKS

The Examiner's Office Action mailed on August 9, 2004 has been received and its contents carefully considered.

Claims 22-40 were previously pending in this application. Claims 22, 28, 29 and 35 are amended, and new claim 41 is added herein. Claims 22, 28 and 35 remain the independent claims in this application.

The applicant acknowledges with appreciation the Examiner's early indication that claims 24, 26, 27, 31, 33, 34, 37, 39 and 40 would be allowable if rewritten in independent form to include all of the limitations of the base claim and any intervening claims.

In the Action, claim 29 is rejected under 35 USC §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the applicant regards as the invention. Specifically, the Examiner asserts that the claim language "detaching the adhesive sheet from the after the ceasing" is not understandable. This is clearly a typographical error. To overcome the rejection, the claim is corrected herein to read "detaching the adhesive sheet from the second surface after the ceasing" (added wording emphasized). Reconsideration and withdrawal of the rejection is respectfully requested.

Claims 22, 23 28, 30, 35 and 36 stand rejected under 35 USC 102(e) as anticipated by Jeong et al. (U.S. Patent No. 6,060,778). Claims 25, 32 and 38 stand rejected under 35 USC 103(a) as obvious over Jeong in view of Egawa et al. (U.S. Patent No. 5, 992, 725). Claims 22, 28 and 35 are amended herein to overcome these rejections.

As recited in amended claims 22 and 35, the present invention teaches a wiring substrate that is thicker than the semiconductor IC chip being mounted in the through hole, such that a difference in height (see application Figure 1, numeral 7) exists between the chip second surface and the substrate second surface when the chip first surface and the substrate first surface are at substantially the same level. This allows the sealing resin coating to flow through the gaps between the side surfaces of the semiconductor IC chip and the through hole in the wiring substrate (see, for example, application at page 3, lines 1-5).

In the Action, the Examiner points to Jeong as disclosing all of the elements of the claimed method. However, as shown in Figure 6, for example, Jeong discloses a wiring

substrate that has a thickness equal to or even somewhat smaller than that of the semiconductor IC chip. As such, any excess sealing resin coating that flows through the gaps between the side surfaces of the semiconductor IC chip and the through hole in the wiring substrate would coat the back surface of the wiring substrate and have to be removed. That is, an extra process step would be required, adding to the time and cost of device fabrication.

In the Action, the Examiner specifically points to Figure 6 of Jeong as specifically disclosing "ceasing the supporting of the semiconductor IC chip (Figure 6, #40) so that the sealing resin (Figure 6, #42) is a substantially sole member for physically connecting the semiconductor IC chip (Figure 6, #40) with the wiring substrate (Figure 6, #32, 38, & 70)." However, contrary to the Examiner's position in this instance, Figure 6 fails to teach or suggest that the sealing resin "is a substantially sole member for physically connecting the semiconductor IC chip." Rather, it appears in Figure 6 of Jeong that heat sink 73, which is permanently bonded to conductive layer 70 by adhesive 72, serves to provide significant mechanical support to the semiconductor IC chip 40, in addition to sealing resin 42.

Amended claim 28 recites that the semiconductor IC chip is put on an adhesive sheet, and that after coating with a sealing resin, the adhesive sheet is removed "so that the sealing resin is a substantially sole member for physically connecting the semiconductor IC chip with the wiring substrate."

To the contrary, Jeong fails to disclose at all or even suggest the use of an adhesive sheet for this purpose. With regard to claim 28, the Examiner points in the Office Action to the through hole 36 as corresponding to the recited "adhesive sheet." With all due respect, this statement is clearly incorrect. If anything, the Examiner would be more likely assert a correspondence between adhesive 72 in Jeong's Figure 6 and the adhesive sheet of claim 28. Even so, Jeong fails to teach or suggest that adhesive 72 is ever removed at any point in the process "to cease the supporting of the semiconductor IC chip," as claim 28 would require. Rather, adhesive 72 clearly appears intended to provide a permanent bond for heat sink 73 (see, for example, Jeong column 20, lines 22-29).

The Egawa reference is relied upon by the Examiner, with regard to claims 25, 32 and 38, to show "the connecting" of the bond pads on the semiconductor IC chip with the conductive lines on the wiring substrate as "including applying conductive paste between

the bond pads and the conductive lines." Egawa is directed to an apparatus for attaching bonding wires to bonding pads on a semiconductor device using a bonding material without applying a dynamic or thermal load to the semiconductor device. Thus, Egawa does not expressly disclose "applying conductive paste between the bond pads and the conductive lines, as the rejected claims require. Moreover, the teaching of Egawa is moot because it does not address any of the deficiencies in the primary reference, Jeong, which have been discussed above. Accordingly, it is respectfully submitted that amended claims 22, 28 and 35, as well as dependent claims 23-27, 29-34 and 36-40, patentably distinguish over the applied prior art references, whether considered individually or in combination.

New dependent claim 41 is added to further recite, in the context of claim 28, the distinguishing features of the invention highlighted in the amendments to claims 22 and 35.

In summary, it is submitted that this Amendment places the application, with claims 22-41, in condition for allowance. Notice of allowance and passing of this application to issue are respectfully requested.

Should the Examiner feel that a conference would help to expedite the prosecution of this application, the Examiner is hereby invited to contact the undersigned counsel to arrange for such an interview.

Respectfully submitted,

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Date

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